WHAT IS CLAIMED IS:

1. A phase-locked loop (PLL) comprising:

a charge-pump loop filter configured to provide a control voltage having a voltage level based on a state of a first charge-pump (CP) control signal and on a state of a second CP control signal; and

a phase detector system configured to receive a first clock having a state, a second clock having a state, and an input signal defining a plurality of states including a first state and a second state, and configured to provide the first CP control signal and the second CP control signal each having a state based on the states of and on a phase difference between the first and second clocks when the input signal has the first state, and to provide the first CP control signal and second CP control signal each having a state asynchronously controlled by the input signal when the input signal has the second state.

2. The PLL of claim 1, wherein the first clock comprises a reference clock and the second clock comprises a feedback clock.

3. The PLL of claim 1, wherein the phase detector system further comprises:

a clock control circuit configured to provide a first output signal having a state substantially equal to the state of the first clock and a second output signal having a state substantially equal to the state of the second clock when the input signal has the first state, to provide the first and second output signals having a state asynchronously controlled by the input signal when the input signal has the second state, and to provide a third output signal having a state based on the first and second CP control signals when the input signal has the first state and a state asynchronously controlled by the input signal when the input signal has the second state; and

a sequential phase-frequency detector (PFD) configured to provide the first CP control signal having a state based on the states of the first and/or third

output signals and the second CP control signal having a state based on the states of the second and/or third output signals.

4. The PLL of claim 3, wherein the clock control circuit comprises a logic circuit configured to minimize propagation delays when the input signal has the first state, and including delay elements configured to prevent phase detector system race-through conditions when the input signal has the second state.

5. The PLL of claim 4, wherein the input signal comprises a first input signal, a second input signal, and a third input signal, each having a first and a second state.

6. The PLL of claim 5, wherein the clock control circuit further comprises:

a reference logic circuit configured to receive the first clock and the first, second, and third input signals, to provide the first output signal having a state equal to the state of the first clock when the first, second, and third input signals each have the first state, to provide the first output signal having a state equal to the state of the first input signal when the first input signal has the second state and the second and third input signals have the first state, and to provide the first output signal having a state equal to the state of the first input signal when the first and third input signals have the first state and the second input signal has the second state.

7. The PLL of claim 5, wherein the clock control circuit further comprises:

a feedback logic circuit configured to receive the second clock and the first, second, and third input signals, to provide the second output signal having a state equal to the state of the second clock when the first, second, and third input signals each have the first state; to provide the second output signal having a state equal to the state of the second input signal when the second input signal has the second state and the first and third input signals have the first state, and to provide the second output signal having a state equal to the state of the second

input signal when the second and third input signals have the first state and the first input signal has the second state.

8. The PLL of claim 5, wherein the clock control circuit further comprises:

a reset logic circuit configured to receive an inverse of each of the first, second, and third input signals, to receive a CP status signal having a state based on the states of the first and second CP control signals, to provide a reset signal having a state substantially equal to the state of the status signal when the first, second, and third input signals each have the first state, to provide the reset signal having a state substantially equal to the state of the third input signal when the third input signal has the second state, and to provide the reset signal having a state substantially equal to the state of the third input signal when the third input signal has the first state and either the fist input signal and/or the second input signal have the second state.

9. The PLL of claim 4, wherein the sequential phase-frequency detector further comprises:

a first D-latch configured to receive the first output signal at a clock input and to provide the first CP control signal at a Q-output;

a second D-latch configured to receive the second output signal at a clock input and to provide the first CP control signal at a Q-output; and

an AND-gate configured to receive the first and second CP control signals at a pair of input terminals and to provide a latch reset signal having a state based on the states of the first and second CP control signals.

10. The PLL of claim 9, wherein the state of the third output signal is substantially equal to the state of latch reset signal when input signal has the first state and a state asynchronously controlled by the input signal when the input signal has the second state.

11. A phase detector system for a phase-locked loop (PLL) including a charge-pump loop filter configured to provide a control voltage having a voltage

level based on a state of a first charge-pump (CP) control signal and on a state of a second CP control signal, the phase detector system comprising:

a clock control circuit configured to receive a first clock having a state, a second clock having a state, and an input signal defining a plurality of states, to provide a first output signal having a state substantially equal to the state of the first clock and a second output signal having a state substantially equal to the state of the second clock when the input signal has the first state, to provide the first and second output signals having a state asynchronously controlled by the input signal when the input signal has the second state, and to provide a third output signal having a state based on the first and second CP control signals when the input signal has the first state and a state asynchronously controlled by the input signal when the input signal has the second state; and

a sequential phase-frequency detector (PFD) configured to provide the first CP control signal having a state based on the states of the first and/or third output signals and the second CP control signal having a state based on the states of the second and/or third output signals.

12. The PLL of claim 11, wherein the first clock comprises a reference clock and the second clock comprises a feedback clock.

13. The PLL of claim 11, wherein the clock control circuit comprises a logic circuit configured to minimize propagation delays when the input signal has the first state, and including delay elements configured to prevent phase detector system race-through conditions when the input signal has the second state.

14. The PLL of claim 13, wherein the input signal comprises a first input signal, a second input signal, and a third input signal, each having a first and a second state.

15. The PLL of claim 14, wherein the clock control circuit further comprises:

a reference logic circuit configured to receive the first clock and the first, second, and third input signals, to provide the first output signal having a state

equal to the state of the first clock when the first, second, and third input signals each have the first state, to provide the first output signal having a state equal to the state of the first input signal when the first input signal has the second state and the second and third input signals have the first state, and to provide the first output signal having a state equal to the state of the first input signal when the first and third input signals have the first state and the second input signal has the second state.

16. The PLL of claim 14, wherein the clock control circuit further comprises:

a feedback logic circuit configured to receive the second clock and the first, second, and third input signals, to provide the second output signal having a state equal to the state of the second clock when the first, second, and third input signals each have the first state; to provide the second output signal having a state equal to the state of the second input signal when the second input signal has the second state and the first and third input signals have the first state, and to provide the second output signal having a state equal to the state of the second input signal when the second and third input signals have the first state and the first input signal has the second state.

17. The PLL of claim 14, wherein the clock control circuit further comprises:

a reset logic circuit configured to receive an inverse of each of the first, second, and third input signals, to receive a CP status signal having a state based on the states of the first and second CP control signals, to provide a reset signal having a state substantially equal to the state of the status signal when the first, second, and third input signals each have the first state, to provide the reset signal having a state substantially equal to the state of the third input signal when the third input signal has the second state, and to provide the reset signal having a state substantially equal to the state of the third input signal when the third input signal has the first state and either the first input signal and/or the second input signal have the second state.

18. The PLL of claim 13, wherein the sequential phase-frequency detector further comprises:

a first D-latch configured to receive the first output signal at a clock input and to provide the first CP control signal at a Q-output;

a second D-latch configured to receive the second output signal at a clock input and to provide the first CP control signal at a Q-output; and

an AND-gate configured to receive the first and second CP control signals at a pair of input terminals and to provide a latch reset signal having a state based on the states of the first and second CP control signals.

19. The PLL of claim 18, wherein the state of the third output signal is substantially equal to the state of latch reset signal when input signal has the first state and a state asynchronously controlled by the input signal when the input signal has the second state.

20. A method of operating a phase-locked loop comprising:

providing a control voltage having a voltage level based on a state of a first charge-pump signal and on a state of a second charge pump signal;

receiving a first clock having a state, a second clock having a state, and an input signal defining a plurality of states including a first state and a second state;

providing the first charge-pump control signal and the second charge-pump control signal, each having a state based on the states of and on a phase difference between the first clock and the second clock; and

controlling the states of the first charge-pump signal and the second charge pump signal asynchronously based on the input signal when the input signal has the second state.

21. The method of claim 20, further comprising:

adjusting a frequency of the second clock based on the control voltage.